GL4H-QDMM85SR8C

QSFP−DD 400Gb/s 850nm 100m MPO Transceiver

PRODUCT FEATURES

• Hot-pluggable QSFP-DD form factor

• Support 400G bps aggregate bit rates

• Up to 53.125G bps Data rate per channel

• Length up to 70m OM3 and 100m OM4 MMF

• MPO-16 APC connector receptacle

• Case temperature range: 0 ~ +60℃

• power dissipation: <12W

• Single 3.3V power supply

APPLICATIONS

• 400GBASE-SR8 400G Ethernet
• Data center interconnection

PRODUCT DESCRIPTION

FIBRECROSS GL4H-QDMM85SR8C is hot-pluggable QSFP-DD transceiver for 400G links over multimode fiber. It is high performance module for short-range data communication and interconnect application which operate at 400Gbps up to 70m using OM3 multi-mode fiber or 100m using OM4 multi-mode fiber. This module is designed to operate over multi-mode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 pins connector. The optical interface uses MPO connector.

Ordering information

Product part Number	Date Rate (Gbps)	Media	Wavelength (nm)	Transmission Distance	Temperature Range（Tcase）（℃）	
GL4H-QDMM85SR8C	400	MMF		70M at OM3 100M at OM4	0~60	Commercial

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	5	85	%
Supply Voltage	Vcc	-0.4	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+60	°C
Supply Voltage	Vcc	3.135	3.3	3.465	V
Supply Current	Icc			3636	mA
Bit Rate	BR		424.96		Gbps
Fiber Length onOM3 MMF				70	m
Fiber Length on OM4 MMF				100	m

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Modulation format			PAM4			
Signaling rate, each lane (range)			26.5625±100ppm		GBd	
Center Wavelength	λ	840		860	nm	
Spectral Width	RMS			0.6	nm	1
Average Launch Power, each lane		-6.5		4	dBm	
Outer Optical Modulation Amplitude, each lane	OMA$_{outer}$	-4.5	-	3	dBm	2
Launch power in OMA$_{outer}$ minus TDECQ	TDECQ	-5.9	-	4.5	dBm	
Average launch power of OFF transmitter, each lane	P$_{off}$			-30	dBm	
Extinction Ratio, each lane	ER	3	-	-	dB	
Optical Return Loss Tolerance	ORL	-	-	-30	dB	
Receiver						
Signaling rate, each lane (range)			26.5625±100ppm		GBd	
Modulation format			PAM4			

Receiver Wavelength	λ	840		860	nm	
Damage threshold		5			dBm	3
Average receive power, each lane		-8.4		4	dBm	4
Receive power(OMAOuter), each lane			-	3	dBm	
Receiver Sensitivity (OMA), each lane	Sen_{OMA}	RS = max (-6.5, SECQ – 7.9)			dB	5
Stressed Receiver Sensitivity (OMA), each lane	Sen_S	-	-	-3.4	dBm	
Receiver Reflectance	RFL	-	-	-12	dB	
Stressed eye closure for PAM4 (SECQ), lane under test			4.5		dB	6
OMA outer of each aggressor lane		-	3		dBm	6

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ < 1.5 dB, the OMA (min) must exceed this value.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5dB.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electrical Characteristics

Transmitter					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Differential Input Voltage Swing	V_{IN}	400	-	900	mV
Tx Differential Input Impendence	Z_{IN}	-	100	-	Ω
Receiver					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Differential output Voltage Swing	V_{OUT}	300	-	900	mV

Pin Description

Top side viewed from top

38 GND	76 GND
37 TX1n	75 TX5n
36 TX1p	74 TX5p
35 GND	73 GND
34 TX3n	72 TX7n
33 TX3p	71 TX7p
32 GND	70 GND
31 InitMode	69 Reserved
30 Vcc1	68 Vcc2
29 VccTx	67 VccTx1
28 IntL	66 Reserved
27 ModPrsL	65 NC
26 GND	64 GND
25 RX4p	63 RX8p
24 RX4n	62 RX8n
23 GND	61 GND
22 RX2p	60 RX6p
21 RX2n	59 RX6n
20 GND	58 GND

Legacy QSFP28 Pads — Additional QSFP-DD Pads

(Module Side) — Module Card Edge (Host Side)

Bottom side viewed from bottom

GND 39	GND 1
TX6n 40	TX2n 2
TX6p 41	TX2p 3
GND 42	GND 4
TX8n 43	TX4n 5
TX8p 44	TX4p 6
GND 45	GND 7
Reserved 46	ModselL 8
VS1 47	ResetL 9
VccRx1 48	VccRx 10
VS2 49	SCL 11
VS3 50	SDA 12
GND 51	GND 13
RX7p 52	RX3p 14
RX7n 53	RX3n 15
GND 54	GND 16
RX5p 55	RX1p 17
RX5n 56	RX1n 18
GND 57	GND 19

Module Card Edge (Host Side)

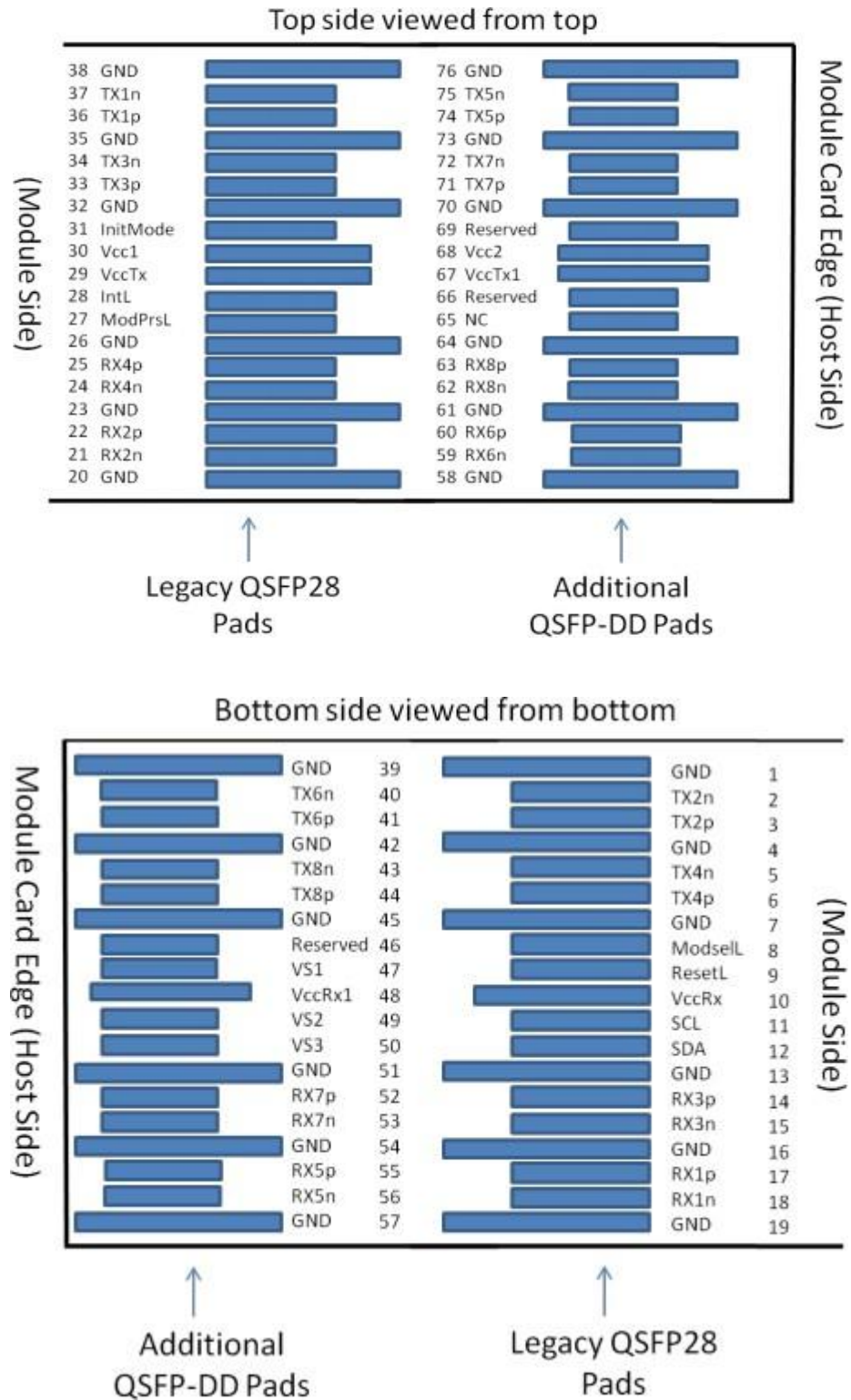Additional QSFP-DD Pads — Legacy QSFP28 Pads

(Module Side)

Diagram of Host Board Connector Block Pin Numbers and Name

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vccl	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1,Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 Kohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

EEPROM Memory Map

CMIS Module Memory Map
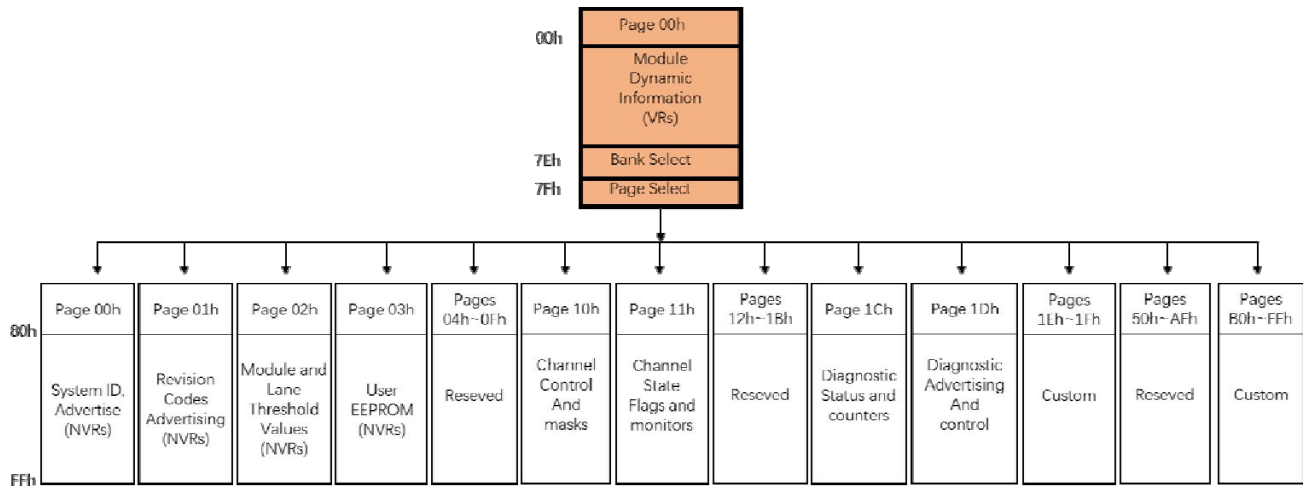
Recommended Interface Circuit

Table 17- Lower Page Overview (Lower Page)

Address	Size	Name	Description
0-1	2	Id and version ID	Module ID from SFF-8024 list, version number, Type and status
2-3	2	Flat mem, CLEI present, TWI speed, Module State, Interrupt	Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Bank Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module Flags	All flags that are module wide (i.e. not lane specific)
14-25	12	Module Monitors	
26-30	5	Module Global Controls	
31-36	6	Module masks	Module flag masks
37-63	27	Reserved	
64-84	21	Custom	
85	1	Module Type advertising code	
86-117	32	Module Host-Media Interface Advertising Options	Host and media interfaces that are supported by the module
118-125	8	Password area	
126	1	Bank Select Byte	
127	1	Page Select Byte	

Table 27- Upper Page 00 Overview (Page 00h)

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Table 37- Upper Page 01 Overview (Page 01h)

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Management Interface features advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-175	13	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
223-250	28	Extended Module Host-Media Interface Advertising options	
251-254	4	Reserved	
255	1	Checksum	Checksum of bytes 130-254[1]

Byte	Size (bytes)	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	
230-254	25	Customizable space	
255	1	Checksum	Covers bytes 128-254

Table 49- Upper Page 02 Overview (Page 02h)

Mechanical Dimensions
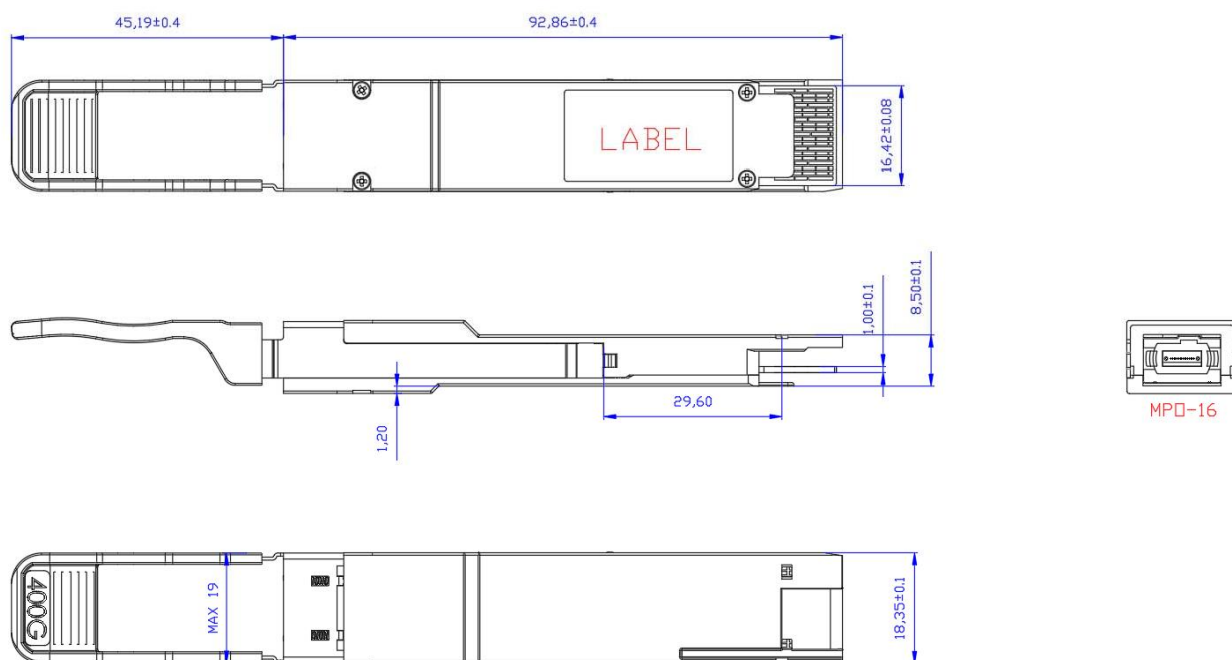
Regulatory Compliance

Agency	Standard	Certificate /Comments
CE-EMC	EN 55032: 2015	17706703 003
	EN 55024: 2010+A1	
REACH	REACH SVHC 197	68.420.19.0344.01
FCC	FCC Rules and Regulations Part 15 Subpart B Class B	MTi190422E141C
RoHS	2011/65/EU and amendment (EU) 2015/863	68.420.17.1030.01