GL4H-OSMM85SR8C

OSFP 400Gb/s 850nm 100m MPO Transceiver

PRODUCT FEATURES

- Hot-pluggable OSFP form factor
- Support 400G bps aggregate bit rates
- Up to 53.125G bps Data rate per channel
- Length up to 70m OM3 and 100m OM4 MMF
- MPO-16 APC connector receptacle
- Case temperature range: 0 ~ +60°C
- power dissipation: <12W
- Single 3.3V power supply

APPLICATIONS

- 400GBASE-SR8 400G Ethernet
- Data center interconnection

PRODUCT DESCRIPTION

Shenzhen Photonics Valley GL4H-OSMM85SR8C is hot-pluggable OSFP transceiver for 400G links over multimode fiber. It is high performance module for short-range data communication and interconnect application which operate at 400Gbps up to 70m using OM3 multimode fiber or 100m using OM4 multimode fiber. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 pins connector. The optical interface uses MPO connector.

Ordering information

Product part Number	Date Rate (Gbps)	Media	Wavelength (nm)	Transmission Distance	Temperature Range （Tcase）（℃）	
GL4H-OSMM85SR8C	400	MMF		70M at OM3 100M at OM4	0~60	Commercial

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	5	85	%
Supply Voltage	Vcc	-0.4	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+60	°C
Supply Voltage	Vcc	3.135	3.3	3.465	V
Supply Current	Icc			3636	mA
Bit Rate	BR	424.96			Gbps
Fiber Length onOM3 MMF				70	m
Fiber Length on OM4 MMF				100	m

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Modulation format	PAM4					
Signaling rate, each lane (range)		26.5625±100ppm			GBd	
Center Wavelength	λ	840		860	nm	
Spectral Width	RMS			0.6	nm	1
Average Launch Power, each lane		-6.5		4	dBm	
Outer Optical Modulation Amplitude, each lane	OMA_{outer}	-4.5	-	3	dBm	2
Launch power in OMA_{outer} minus TDECQ	TDECQ	-5.9	-	4.5	dBm	
Average launch power of OFF transmitter, each lane	P_{off}			-30	dBm	
Extinction Ratio, each lane	ER	3	-	-	dB	
Optical Return Loss Tolerance	ORL	-	-	-30	dB	
Receiver						
Signaling rate, each lane (range)		26.5625±100ppm			GBd	
Modulation format		PAM4				
Receiver Wavelength	λ	840		860	nm	

Damage threshold		5			dBm	3
Average receive power, each lane		-8.4		4	dBm	4
Receive power(OMAOuter), each lane			-	3	dBm	
Receiver Sensitivity (OMA), each lane	Sen_{OMA}	RS = max (-6.5, SECQ – 7.9)			dB	5
Stressed Receiver Sensitivity (OMA), each lane	Sen_S	-	-	-3.4	dBm	
Receiver Reflectance	RFL	-	-	-12	dB	
Stressed eye closure for PAM4 (SECQ), lane under test			4.5		dB	6
OMA outer of each aggressor lane		-	3		dBm	6

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ < 1.5 dB, the OMA (min) must exceed this value.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5dB.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electrical Characteristics

Transmitter					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Differential Input Voltage Swing	V_{IN}	400	-	900	mV
Tx Differential Input Impendence	Z_{IN}	-	100	-	Ω
Receiver					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Differential output Voltage Swing	V_{OUT}	300	-	900	mV

Pin Description

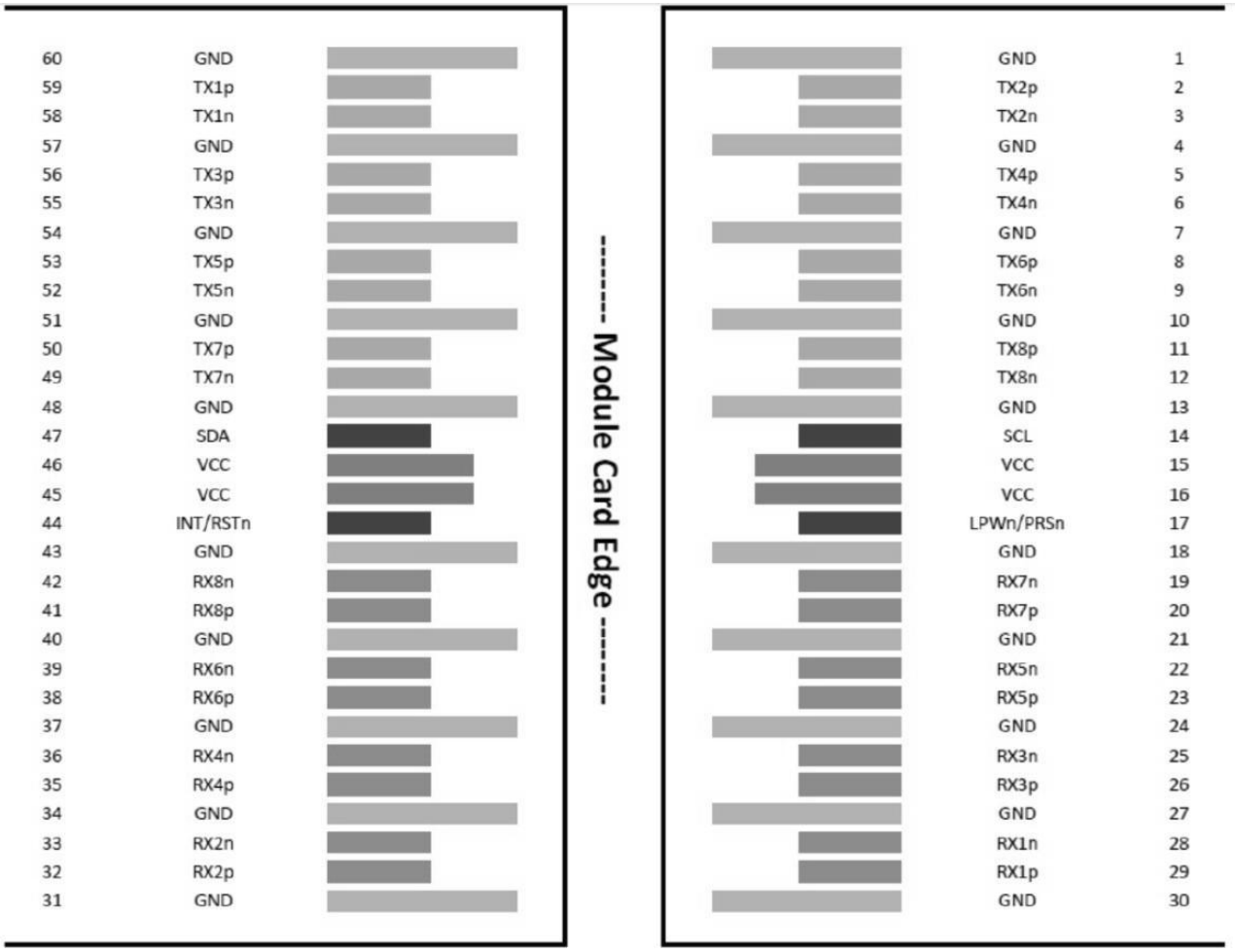


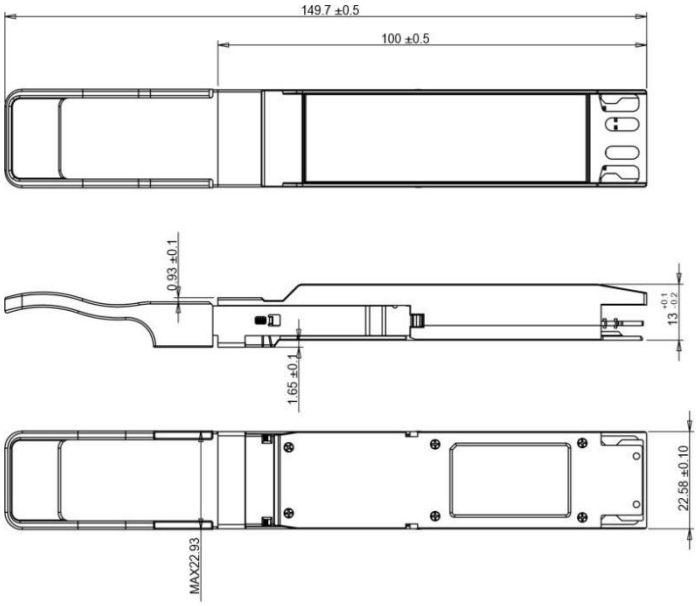
Diagram of Host Board Connector Block Pin Numbers and Name

Pin No.	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O	Bi-directional	3
15	V_{CC}	+3.3V Power		Power from Host	2
16	V_{CC}	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3

Pin No.	Symbol	Description	Logic	Direction	Plug Sequence
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1

Pin No.	Symbol	Description	Logic	Direction	Plug Sequence
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3
45	V_{CC}	+3.3V Power		Power from Host	2
46	V_{CC}	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Mechanical Dimensions



Regulatory Compliance

Agency	Standard	Certificate /Comments
CE-EMC	EN 55032: 2015	17706703 003
	EN 55024: 2010+A1	
REACH	REACH SVHC 197	68.420.19.0344.01
FCC	FCC Rules and Regulations Part 15 Subpart B Class B	MTi190422E141C
RoHS	2011/65/EU and amendment (EU) 2015/863	68.420.17.1030.01